

What is Claimed is:

- [c1] 1. A method of designing an integrated circuit chip, said method comprising:
- supplying a chip design;
 - partitioning elements of said chip design according to similarities in voltage requirements and timing of power states of said elements to create voltage islands;
 - outputting a voltage island specification list comprising at least one of power, simulation, reliability, floorplanning, and timing information of each voltage island; and
 - simulating said chip design using an unknown voltage state propagation on voltage island cell outputs identified by a power-on/off control signal within said voltage island specification list.
- [c2] 2. The method in claim 1, further comprising performing a static timing analysis using minimum, maximum, and nominal voltages for each island from said voltage island specification list.
- [c3] 3. The method in claim 2, wherein said performing of said static timing analysis comprises, for paths communicating between two islands, using minimum-to-minimum, maximum-to-maximum, minimum-to-maximum, and maximum-to-minimum voltage values from said voltage island specification list to measure and optimize timing.
- [c4] 4. The method in claim 1, further comprising performing a power calculation utilizing power-on hours and a percent-on factor for each island from said voltage island specification list.
- [c5] 5. The method in claim 1, further comprising testing each island individually and said chip design as a whole.
- [c6] 6. The method in claim 1, wherein said simulating comprises using a test bench to force said voltage island cell outputs to said unknown states when said control signal indicates said power-off condition.
- [c7] 7. The method in claim 1, wherein said specification list comprises at least one of a power source name, a power source type, minimum voltage level,

maximum voltage level, nominal voltage level, switching signal name, switching signal type, power on hours, and steady state on percentage.

- [c8] 8. A method of designing an integrated circuit chip, said method comprising:
- supplying a chip design;
 - partitioning elements of said chip design according to similarities in voltage requirements and timing of power states of said elements to create voltage islands;
 - outputting a voltage island specification list comprising power and timing information of each voltage island; and
 - automatically, and without user intervention, synthesizing power supply networks for said voltage islands.
- [c9] 9. The method in claim 8, further comprising performing physical placement of circuit elements on said integrated circuit chip according to a hierarchy established in said voltage island specification list.
- [c10] 10. The method in claim 9, wherein during said physical placement processing, limits are placed upon inserting logic elements within said voltage islands.
- [c11] 11. The method in claim 8, further comprising performing routing physical wiring within said integrated circuit chip according to a hierarchy established in said voltage island specification list.
- [c12] 12. The method in claim 8, further comprising constraining placement of physical pins to edges of said voltage islands adjacent power rings of a power supply within said integrated circuit chip.
- [c13] 13. The method in claim 8, wherein said specification list comprises at least one of a power source name, a power source type, minimum voltage level, maximum voltage level, nominal voltage level, switching signal name, switching signal type, power on hours, and steady state on percentage.
- [c14] 14. A program storage device readable by machine, tangibly embodying a program of instructions executable by said machine for performing a method of designing an integrated circuit chip, said method comprising:

supplying a chip design;
partitioning elements of said chip design according to similarities in
voltage requirements and timing of power states of said elements to
create voltage islands;
outputting a voltage island specification list comprising power and timing
information of each voltage island; and
simulating said chip design using an unknown voltage state on inputs of a
voltage island when a timing waveform within said voltage island
specification list indicates a power-off condition within said voltage
island.

- [c15] 15. The program storage device in claim 14, wherein said method further comprises performing a static timing analysis using minimum, maximum, and nominal voltages for each island from said voltage island specification list.
- [c16] 16. The program storage device in claim 15, wherein said performing of said static timing analysis comprises, for paths communicating between two islands, using minimum-to-minimum, maximum-to-maximum, minimum-to-maximum, and maximum-to-minimum voltage values from said voltage island specification list to measure and optimize timing.
- [c17] 17. The program storage device in claim 14, further comprising performing a power calculation utilizing power-on hours and a percent-on factor for each island from said voltage island specification list.
- [c18] 18. The program storage device in claim 14, further comprising testing each island individually and said chip design as a whole.
- [c19] 19. The program storage device in claim 14, wherein said simulating comprises using a test bench to force said inputs to said unknown states when said control signal indicates said power-off condition.
- [c20] 20. The program storage device in claim 14, wherein said specification list comprises at least one of a power source name, a power source type, minimum voltage level, maximum voltage level, nominal voltage level, switching signal name, switching signal type, power on hours, and steady state on percentage.